High Mobility Si/SiGe Strained Channel MOS Transistors with HfO_2/TiN Gate Stack

S. Datta, G. Dewey, M. Doczy, B.S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar,
M. Metz, N. Zelick and R. Chau

Components Research, Intel Corporation, Hillsboro, OR-97124, USA

Abstract

We integrate strained Si channel with HfO_2 dielectric and TiN metal gate electrode to demonstrate NMOS transistors with electron mobility better than the universal mobility curve for SiO_2, inversion equivalent oxide thickness of 1.4nm (EOT=1nm), and with three orders of magnitude reduction in gate leakage. To understand the physical mechanism that improves the inversion electron mobility at the HfO_2/strained Si interface, we measure mobility at various temperatures and extract the various scattering components.

Introduction

HfO_2 is one of the most promising high-k candidates to replace SiON as a gate dielectric in future generations of CMOS technology due to its large band offsets, thermodynamic stability in contact with Si (1), and excellent high-frequency response (2). However, the most serious drawback in integrating HfO_2 as an alternate gate dielectric in today's Si CMOS transistors is the 40-50% degradation in electron mobility with HfO_2/Poly-Si gate stacks (3). In this paper, we integrate for the first time strained Si channel on relaxed Ge_xSi_{1-x} (Ge=10%) virtual substrate, HfO_2 gate dielectric directly on strained Si, and TiN metal gate in a conventional CMOS flow to demonstrate NMOS transistors with 35% higher mobility than the unstrained Si control with HfO_2/TiN gate. These high-k gate stacks with TiN gate electrode achieve inversion equivalent oxide thickness (T_{inv}) of 1.4nm and EOT = 1nm, with 3 orders of magnitude lower gate leakage than the SiON control. Furthermore, to understand the various physical scattering mechanisms that limit electron mobility at the HfO_2/Si interface, we experimentally measure the effective inversion electron mobility as a function of temperature and transverse electric field (E_{eff}) for various gate stacks, and conclude that surface phonon scattering is the primary cause of electron mobility degradation with HfO_2 dielectrics. We also show experimentally that the TiN metal gate screening effect and the biaxial tensile strain in the channel help improve the overall HfO_2 surface phonon limited mobility significantly, without the need for a thick buffer SiO_2 or SiON layer between the HfO_2 and the Si substrate, thereby achieving high electron mobility and low T_{inv} at the same time.

Experimental Results

NMOS transistors were fabricated integrating strained Si channel with HfO_2 dielectric and TiN gate electrode. Fig. 1 shows a schematic illustration of the device structure. A thin layer of tensile-strained Si is deposited on a 1.5um thick layer of compositionally graded and fully relaxed Ge_xSi_{1-x} by UHVCVD process. Following shallow trench isolation and well implants, an ultra thin HfO_2 layer is deposited directly on strained Si, followed by TiN and poly-Si deposition processes. Control devices were fabricated at the same time on conventional Si substrate (control Si) with HfO_2 and TiN gate stack, and also with a 1.2 nm thick conventional SiON gate oxide (4). Fig. 2 shows the Raman characterization of the biaxial tensile strain in the ultra-thin strained Si cap layer, which shows an in-plane strain of 0.35%. Fig. 3 shows the cross-sectional TEM image of the strained Si channel on the relaxed $Ge_{.10}Si_{.90}$ virtual substrate. After gate definition and patterning, the transistor fabrication process was completed using source/drain extension implants, halo implants, spacer formation, source/drain implants, activation anneal, and Ni silicidation.

Fig. 4 shows the high frequency split CV measurements on the HfO_2 gate stacks, which yield inversion thickness (T_{inv}) of 1.4nm (including QM effects) on both strained Si and control Si, with negligible hysteresis. In comparison, the SiON control T_{inv} is 1.9 nm due to additional poly-depletion effects. Fig. 5 shows that 1000× reduction in gate leakage is achieved with the HfO_2 gate stacks on both strained Si and control Si. Fig. 6 shows the long channel Id-Vg characteristics for HfO_2/TiN gate stacks on both strained Si and control Si, which shows excellent sub-threshold slope (S.S) values = 66mV/dec, indicating negligible interface states (Dit). Vt shift is from the TiN work-function (= 4.65eV), which is extracted from the intercept of the flat-band voltage (V_{FB}) versus accumulation electrical thickness (T_{acc}) plot (Fig. 7) and not from additional fixed charge (Q_{ss}=7X10^{11}/cm^2 as estimated from the slope). Fig. 6 also shows the long channel Vt reduction by 50mV with strained Si compared to the control. Effective inversion electron mobility was measured on long channel devices on all the gate stacks as shown in Fig. 8 from the I-V and split C-V measurements. For the HfO_2 and TiN gate stack devices, biaxial tensile strain in Si provides 43% peak mobility improvement and 35% enhancement at 1MV/cm E_{eff}, over unstrained control Si devices. Fig.'s 9 and 10 show the Id-Vg and the Id-Vds characteristics of the two devices for Lg=140nm. Both devices exhibit excellent S.S values (indicating negligible D_{it}) and DIBL characteristics. Strained Si devices show Idsat gain of 24% (without self-heating correction) and Idlin gain of 40% over the control Si devices for the same gate over-drive. Strained Si devices with HfO_2 + TiN gate were fabricated down to 80nm gate lengths, as shown in Fig's 11 and 12,

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which show excellent sub-threshold characteristics (S.S.=72mV/dec, DIBL=49mV/V), and I_{on}= 930 μA/μm at I_{off}=1pA/μm at 1.5V Vds for Vgs-Vt=1V.

HfO_2 vs SiON Mobility Analysis

To identify the physical mechanism that degrades inversion electron mobility at HfO_2/Si interface compared to SiON, with poly-Si and TiN metal gate, we measured the effective electron mobility as a function of temperature and E_{eff}, as shown in Fig. 13. Physical models such as acoustic surface phonon scattering, surface roughness scattering, remote and interface fixed oxide charge scattering, channel impurity scattering, bulk phonon scattering, and remote surface optical phonon scattering, as a function of temperature and E_{eff}, were included following Mathiessen's Rule to fit the empirical data (shown by dashed lines in Fig. 13). Various mobility components were extracted for the HfO_2 and the SiON gate stacks, and compared. Fig. 14 shows that the devices with HfO_2 and TiN as well as poly-Si gate show more degradation in surface phonon limited mobility compared to SiON at room temperature. This additional surface phonon induced degradation is from the coupling of the low energy surface optical (SO) phonon modes arising from the polarization of the HfO_2 to the inversion channel electrons (5). Fig. 14 also shows that for a given HfO_2 thickness, TiN metal gate (with higher free electron concentration in the gate, $n_g \sim 10^{21}$ cm^{-3}, and higher plasmon frequency) is more effective in dynamically screening the HfO_2 SO phonons from coupling to the channel electrons under inversion conditions, whereas depleted poly-Si gate (with lower free electron concentration, n_g, and lower plasmon frequency) is less effective. Additional improvement of about 35% in surface phonon limited electron mobility is observed from the biaxial tensile strain in the Si channel with the HfO_2/TiN gate. Fig. 15 shows the simulation results of the reduction of the various phonon scattering processes with increasing biaxial tensile strain with increased Ge concentration, at inversion sheet carrier concentration, n_s, of 10^{13} cm^{-2}. SO phonon scattering limited mobility improves with strain because of the improvement in transport mass from the repopulation of the valleys with lower in-plane mass, and, hence, it saturates for higher Ge %. Inter-valley phonon scattering also improves from the energy splitting of the equivalent valleys in the conduction band due to strain (6).

Summary

In summary, we have successfully demonstrated the integration of strained Si with HfO_2 and TiN metal gate to demonstrate NMOS transistors with electron mobility better than the universal mobility curve at 1MV/cm E_{eff}, ultra-thin high-k gate stack with T_{inv} of 1.4nm and with 3 orders of magnitude reduction in gate leakage. To our knowledge, this is the highest long channel inversion electron mobility demonstrated with HfO_2/TiN gate stack, with a T_{inv} of 1.4nm, without the use of any intentional SiON interfacial buffer layer, as shown in Fig.16. This study also shows experimentally a) the existence of additional phonon scattering mechanism in degrading electron mobility at the HfO_2/Si interface through a temperature sensitivity study; b) the beneficial effect of metal gate electrode screening on the remote phonon-electron interaction, and, finally, c) the role of biaxial tensile strain in the channel in both SO phonon and inter-valley phonon limited mobility improvement.

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Fig. 1 A schematic of strained Si NMOS transistor with HfO_2 dielectric + TiN metal gate.

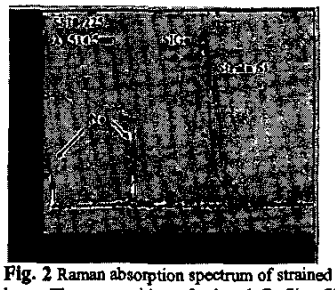

Fig. 2 Raman absorption spectrum of strained Si layer. The composition of relaxed Ge_xSi_{1-x} film from Si-Si Raman peak is 10.1+/-0.3%. In-plane tensile strain in Si cap layer is 0.35+/-0.02%. This agrees well with the lattice mismatch strain based on a_{Si}= 5.43A , a_{Ge}= 5.65 and $a_{Ge_xSi_{1-x}}$ based on Vegard's law, indicating that the Ge_xSi_{1-x} films are fully relaxed and Si cap layers are strained.

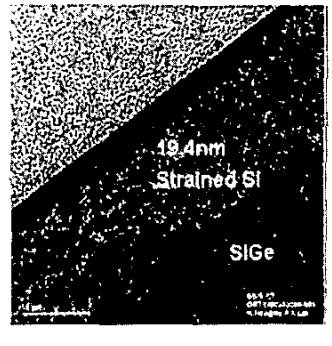

Fig. 3 Cross-section TEM image of the biaxial tensile strained Si layer on relaxed $Ge_{.10}Si_{.90}$ virtual substrate.

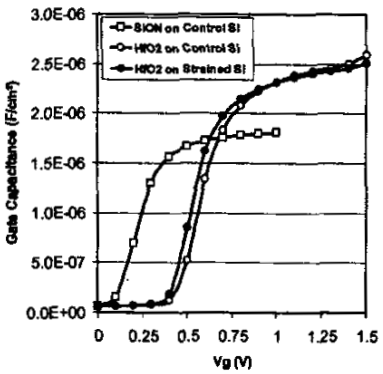

Fig. 4 High frequency split CV measurements of gate to source/drain capacitance for various stacks with negligible hysteresis.

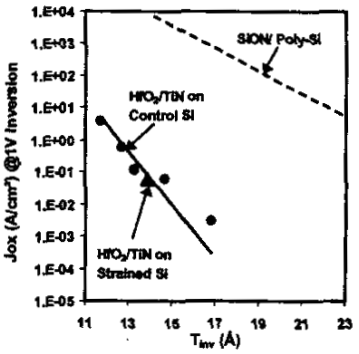

Fig. 5 Gate leakage as a function of T_{inv} for HfO_2 for both Poly-Si and TiN gate electrodes. Also shown is SiON line for reference. Difference in slopes is due to the conduction band offset difference between HfO_2 (~1.5eV) vs SiON (~ 3eV).

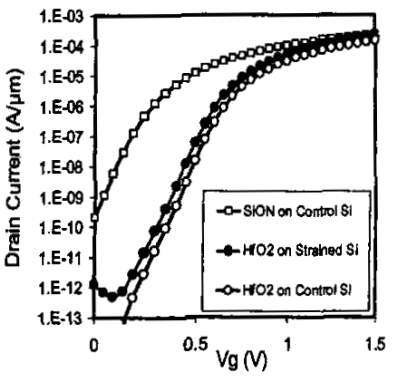

Fig. 6 Long channel (10µm ×10µm) Id-Vg characteristics of HfO_2 on Strained Si + Control Si NFET's.

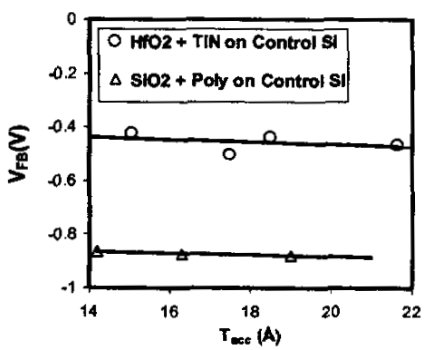

Fig. 7 Flat-band voltage vs accumulation oxide thickness shows that fixed charge concentration in HfO_2/TiN stack is of same order of magnitude (10^{11}/cm^2) as that in SiON/Poly-Si. Work function of TiN on HfO_2 is extracted from the intercept to be ~ 4.65eV.

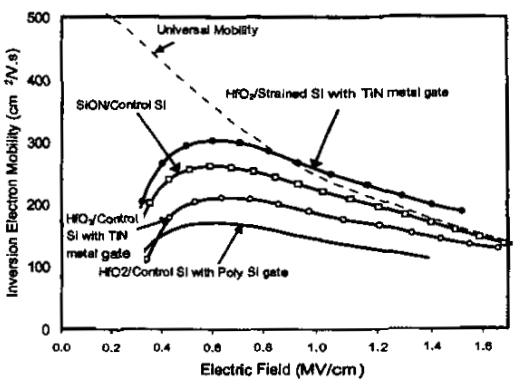

Fig. 8 Electron Mobility as a function of transverse effective electric field (E_{eff}). At 1MV/cm E_{eff}, HfO_2/TiN on control Si device shows mobility degradation by only 15% from the SiON control. HfO_2/TiN on strained Si shows 15% enhancement over SiON control. In contrast, HfO_2/Poly-Si on control Si shows 40% degradation with respect to SiON/Poly-Si gate stack.

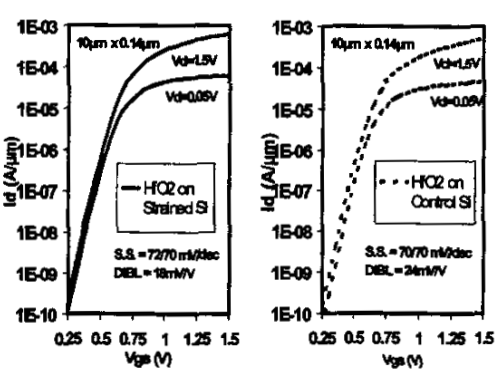

Fig. 9 Id-Vg characteristics of the 140nm HfO_2/TiN NMOS devices on strained Si and on Control Si. Both devices have matched I_{off}, and show excellent S.S. slopes and DIBL values.

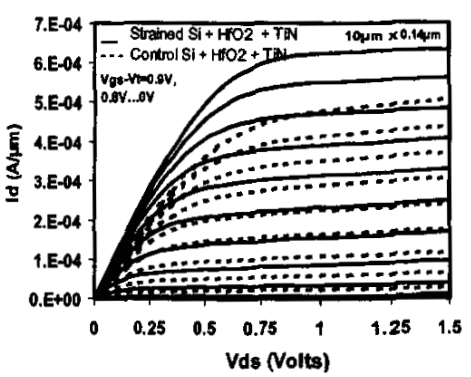

Fig. 10 Id-Vg characteristics of the 140 nm HfO_2/TiN NMOS devices on strained Si and on Control Si. Strained Si devices show 40% Idlin gain and 24% Idsat gain at Vcc=1.5V.

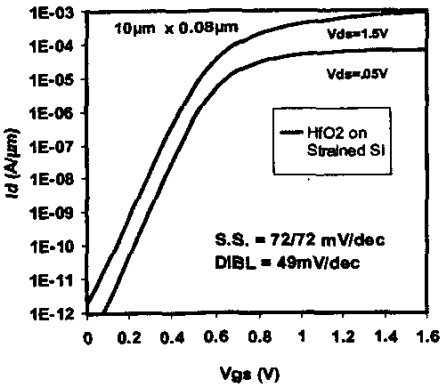

Fig. 11 Id-Vg characteristics of the 80 nm HfO_2/TiN NMOS devices on strained Si showing Ion of 930µA/µm at 1.5V Vds with Ioff of 1pA/um.

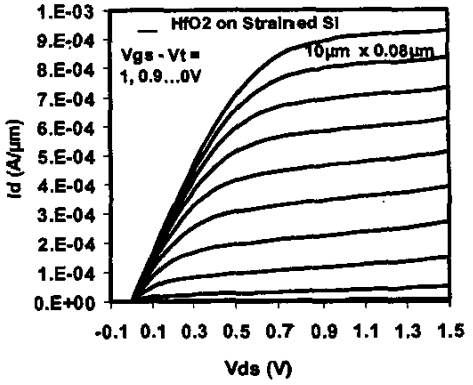

Fig. 12 Id-Vds characteristics of the 80 nm HfO_2/TiN NMOS devices on strained Si (without self-heating correction).

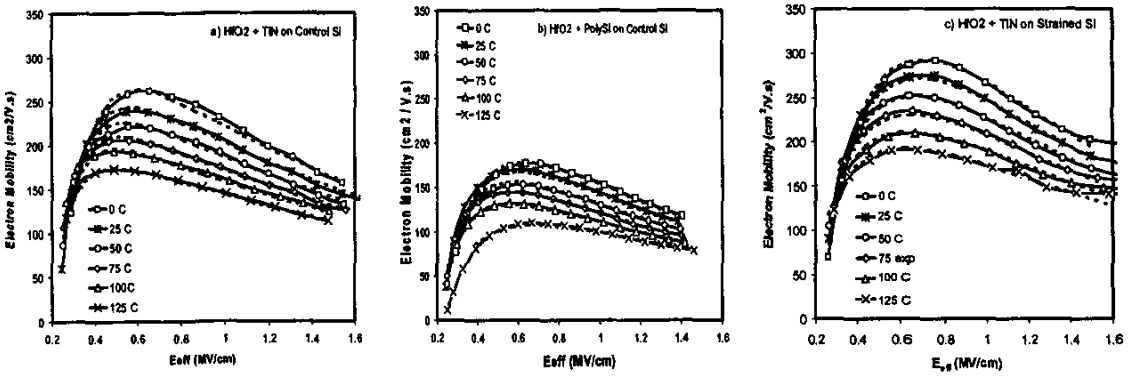

Fig. 13 Experimental (symbols) and fitted data based on physical models (dashed lines) as a function of temperature for a) HfO_2 + TiN metal gate on Control Si, b) HfO_2 + Poly-Si gate on Control Si and c) HfO_2 + TiN metal gate on Strained Si .

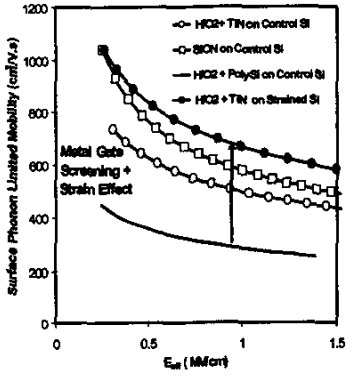

Fig. 14 Surface phonon limited mobility component extracted for HfO_2+TiN metal gate, HfO_2+PolySi on Control Si and HfO_2 + TiN + Strained Si and compared to that for SiON+Poly-Si.

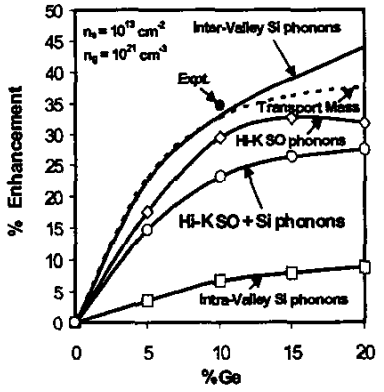

Fig. 15 Simulation of SO phonon mobility enhancement with strain due to reduction in transport mass. Inter-valley phonon scattering also improves from splitting of equivalent valleys in the conduction band.

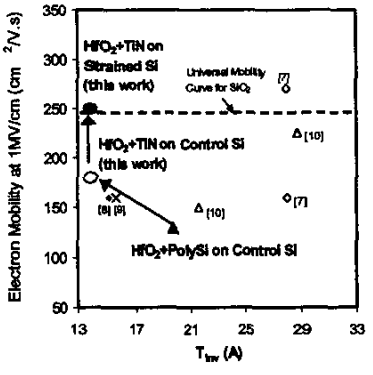

Fig. 16 Inversion electron mobility at 1MV/cm E_{eff} vs T_{inv}. This work achieves high electron mobility for the thinnest T_{inv} reported, through the combination of strained Si channel and HfO_2/TiN gate stack.